

REMARKS

The Office Action dated September 14, 2006 has been received and carefully noted. The above amendments to claims 1, 11-12, 14-16, 20, 25, 26, 27, 31, 35, 37, 40, 41, and 42 and the following remarks are submitted as a full and complete response thereto. Support for the amended recitations may be found, at least, on pages 77-78 of the specification. No new matter is being presented, and approval and entry are respectfully requested. As will be discussed below, it is also requested that all of claims 1-3, 5-12, 14-23, 25-35, 37-38 and 40-42 be found allowable as reciting patentable subject matter.

Claims 1-3, 5-12, 14-23, 25-35, 37-38 and 40-42 stand rejected and pending and under consideration.

REJECTION UNDER 35 U.S.C. § 103:

In the Office Action, at page 2, claims 1-3, 6-12, 14-23, 25-35, 37-38 and 40-42 were rejected under 35 U.S.C. § 103 as being unpatentable over U. S. Patent No. 6,246,680 to Muller et al. ("Muller") in view of U.S. Patent No. 6,999,452 to Murray et al. ("Murray"). The Office Action took the position that Muller and Murray describe all the recitations of independent claims 1, 14, 15, 16, 20, 25, 26, 27, 31, 35, 37, 40, and 41 and related dependent claims. It is respectfully asserted that, for at least the reasons provided herein below, Muller and Murray fail to teach or suggest the recitations of the pending claims. Reconsideration is requested.

Independent claim 1, upon which claims 2, 3, and 5-12 are dependent, recites a network switch, the network switch including at least one data port interface supporting a plurality of data ports, a submodule adding an interstack tag into data to keep track of a stack count to prevent looping of the data, at least one stack link interface comprising a bi-directional gigabit stack link interface configured to transmit the data between said network switch and other network switches to create a predetermined configuration. The data is removed from said at least one stack link interface in a reverse order from that in which the data is added, where the most recently added data is the first one removed. A memory management unit is in communication with the at least one data port interface and the at least one stack link interface, and a memory interface in communication with the at least one data port interface, the ethernet controller, and the at least one stack link interface. The memory interface is configured to communicate with a memory. The memory management unit is configured to route data received from each of the at least one data port interface and the at least one stack link interface to the memory interface.

Independent claim 14, upon which claims 21-23 are dependent, recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data, a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data, a predetermined number of stack link interfaces comprising bi-directional

gigabit stack link interfaces configured to transmit the data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a predetermined configuration. The data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed. A memory management unit is in communication with the at least one data port interface and the predetermined number of stack link interfaces, and a memory interface in communication with the at least one data port interface and the predetermined number of stack link interfaces. The memory interface is configured to communicate with a memory.

Claim 15 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data, a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data, a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a predetermined configuration. The data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, and the predetermined number of stack link

interfaces is configured to be one less than the predetermined number of switch building blocks.

Claim 16 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data, a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data, a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a predetermined configuration. The data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, and the at least one data port interface further includes at least one first data port interface supporting a plurality of first data ports transmitting and receiving data at a first data rate, and at least one second data port interface supporting at least one second data port transmitting and receiving data at a second rate.

Claim 20 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building

blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data, a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data, a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a predetermined configuration. The data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, and each of the predetermined number of stack link interfaces further include a gigabit stack link interface configured to transmit and receive data from another gigabit stack link interface on another switch building block.

Claim 25 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data, a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data, and a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a predetermined configuration. The data is removed from said predetermined number of stack link

interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, a memory management unit in communication with the at least one data port interface and the predetermined number of stack link interfaces, and a memory interface in communication with the at least one data port interface and the predetermined number of stack link interfaces. The memory interface is configured to communicate with a memory.

Claim 26 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data, a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data, a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a predetermined configuration. The data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, and the predetermined number of stack link interfaces is configured to be one less than the predetermined number of switch building blocks.

Claim 27 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data, a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data, a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a predetermined configuration. The data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, and the at least one data port interface further includes at least one first data port interface supporting a plurality of first data ports transmitting and receiving data at a first data rate, and at least one second data port interface supporting at least one second data port transmitting and receiving data at a second rate.

Claim 31 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data, a submodule adding an interstack tag into the data to

keep track of a stack count to prevent looping of the data, a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a predetermined configuration. The data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed, and each of the predetermined number of stack link interfaces further include a gigabit stack link interface configured to transmit and receive data from another gigabit stack link interface on another building block.

Claim 35 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data, a submodule adding an interstack tag into the data to keep track of a stack count to prevent looping of the data, and a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit the data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a predetermined configuration, the scalable network switch further comprising a physical layer transceiver in connection with at least one of the plurality of data ports. The data is removed from

said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed.

Claim 37 recites a method of stacking network switches, the method including providing a plurality of clustered switch blocks, and interconnecting each one of the plurality of clustered switch blocks to another one of the plurality of clustered switch blocks. Interconnection of the plurality of clustered switch blocks forms a stack of clustered switch blocks. The providing of the plurality of clustered switch blocks further includes providing a predetermined number of switch building blocks, interconnecting each of the predetermined number of switch building blocks to every other one of the predetermined number of switch building blocks in a meshed configuration, adding an interstack tag into data received to keep track of a stack count to prevent looping of the data. Each of the predetermined number of switch building blocks is interconnected to every other one of the predetermined number of switch blocks through an individual stack link. The method further removes the data from said individual stack link interface in a reverse order from that in which the data is added, where the most recently added data is the first one removed.

Claim 40 recites a method of stacking network switches, the method including providing a plurality of clustered switch blocks, and interconnecting each one of the plurality of clustered switch blocks to another one of the plurality of clustered switch blocks. Interconnection of the plurality of clustered switch blocks forms a stack of clustered switch blocks, receiving a packet on at least one of a data port interface and a

stack link interface, adding an interstack tag into the packet to keep track of a stack count to prevent looping of the packet, and storing the packet in a memory in accordance with a predetermined algorithm by allocating memory locations in an internal memory and in an external memory based upon an amount of internal memory available for an egress port of the clustered network switch from which the packet is to be transmitted. The method further removes the data from said individual stack link interface in a reverse order from that in which the data is added, where the most recently added data is the first one removed.

Claim 41, upon which claim 42 is dependent, recites a method of stacking network switches, the method including providing a plurality of clustered switch blocks, and interconnecting each one of the plurality of clustered switch blocks to another one of the plurality of clustered switch blocks. Interconnection of the plurality of clustered switch blocks forms a stack of clustered switch blocks, receiving a packet, adding an interstack tag into the packet to keep track of a stack count to prevent looping of the packet, determining if the destination address of the packet corresponds to a port in the clustered network switch, forwarding the packet to the port corresponding to the destination address if the destination address is determined to correspond to a port in the clustered network switch, determining if the destination address of the packet corresponds to a port on another clustered network switch across a stack, forwarding the packet to a stack link if the destination address is determined to correspond to a port on the another clustered network switch across the stack and transmitting the packet across the stack to the

another clustered network switch if the destination address of the packet corresponds to a port on the another clustered network switch across the stack. The method further removes the data from said individual stack link interface in a reverse order from that in which the data is added, where the most recently added data is the first one removed.

As will be discussed below, Muller and Murray fail to disclose or suggest the elements of any of the presently pending claims.

Muller provides that a number of external ports (not shown) having input and output capability interface the external connections 117 are provided. Each subsystem supports multiple Gigabit Ethernet ports, Fast Ethernet ports and Ethernet ports. Internal ports (not shown) also having input and output capability in each subsystem couple the internal links 141. Using the internal links, the MLDNE can connect multiple switching elements together to form a multigigabit switch. However, Muller fails to teach or suggest, at least, “the data is removed from said at least one stack link interface in a reverse order from that in which the data is added, where the most recently added data is the first one removed,” as recited in independent claim 1. Muller does not teach or suggest in either FIG. 2 or corresponding description that the configuration provided therein includes a stack link interface in which the data would be removed from therefrom in a reverse order from that in which the data is added, where the most recently added data is the first one removed. Although Muller provides that the ports have input and output capabilities, that alone does not teach or suggest that the interfaces used in Muller’s configuration provides a bi-direction gigabit stack link interface in which the

data is removed in a reverse order from that in which the data is added, where the most recently added data is the first one removed. Also, Muller's configuration does not create a full duplex configuration.

Independent claims 14-16, 20, 25-27, 31, and 35 recite, at least, "a the data is removed from said predetermined number of stack link interfaces in a reverse order from that in which the data is added, where the most recently added data is the first one removed." Because independent claims 14-16, 20, 25-27, 31, and 35 include similar claim features as those recited in independent claim 1, although of different scope, and because the Office Action refers to similar portions of the cited references to reject independent claims 14-16, 20, 25-27, 31, and 35, the arguments presented above supporting the patentability of independent claims 14-16, 20, 25-27, 31, and 35 are incorporated herein to support the patentability of independent claim 1.

Furthermore, the office action indicates that in column 4, lines 10-15, Muller describes, "each of said predetermined number of switch building blocks is interconnected to every other one of said predetermined number of switch blocks through an individual stack link; and removing the data from said individual stack link interface in a reverse order from that in which the data is added, where the most recently added data is the first one removed," as recited in part in independent claim 37. However, the referred portion of Muller merely describes that in FIG. 2, Ethernet packets may enter or leave the network switch element 100 through any one of the three interfaces 205, 215, or 225. There is nothing in Muller that describes or illustrates in FIG. 2 how the data is

removed from a stack link interface. There is no description or suggestion in Muller of providing an individual stack link interconnecting every other one of the switch blocks. By simply indicating that three interfaces are provided in which, through one of such interfaces, the Ethernet packets may enter or leave, does not teach or suggest the particular recitations of the configuration recited in independent claim 37.

Furthermore, the Office Action correctly recognized that Muller fails to teach or suggest, “a submodule adding an interstack tag into data to keep track of a stack count to prevent looping of the data,” as recited in independent claim 1. Accordingly, the Office Action relied on Murray as curing the deficiencies of Muller.

Murray generally describes a packet-switched network system including a multiplicity of multi-port network units having first and second ports and transmission links to support duplex transmission of Ethernet data packets. Each unit transmits from the first and second ports data including selected information enabling on reception of a packet at any of the units a determination of a number of hops from unit to unit around said ring said packet has made. Each unit has a forwarding database and in response to the said selected information controls the transmission of said packets in two directions around.

Column 7, lines 37-40, of Murray simply describes that if a packet is received on ring port 1 and the number of hops indicated or computed for that packet is equal to the perimeter of the ring, the packet must be discarded. This has no counterpart in 802.1D functionality. However, Murray does not teach or suggest that the data is removed from

the cascading interface 225 in a reverse order from that in which the data is added, where the most recently added data is the first one removed. There is no teaching or suggestion in Murray of the removal of data from a stack link interface as recited in independent claim 1. Thus, clearly and contrary to the contentions made in the Office Action, Murray does not cure the deficiencies of Muller. A combination of Muller and Murray would be devoid of any teaching or suggestion providing that “the data is removed from said at least one stack link interface in a reverse order from that in which the data is added, where the most recently added data is the first one removed,” as recited in independent claim 1. Accordingly, Muller and Murray fail to teach or suggest all the recitations of independent claim 1 and related dependent claims.

Because independent claims 14-16, 20, 25-27, 31, 35, 37, 40, and 41 recite similar claim features as those recited in independent claim 1, although of different scope, and because the Office Action refers to similar portions of the cited references to reject independent claims 14-16, 20, 25-27, 31, 35, 37, 40, and 41, the arguments presented above supporting the patentability of independent claim 1 are incorporated herein to support the patentability of independent claims 14-16, 20, 25-27, 31, 35, 37, 40, and 41.

Accordingly, for the foregoing reasons, it is respectfully requested that the rejection of claims 1-3, 6-12, 14-23, 25-35, 37-38 and 40-42 be withdrawn.

REJECTION UNDER 35 U.S.C. § 103:

In the Office Action, at page 11, claim 5 was rejected under 35 U.S.C. § 103 as being unpatentable over Muller, Murray, and U.S. Patent No. 6,775,290 to Merchant et al. (“Merchant”). The Office Action took the position that Muller, Murray, and Merchant discloses all the aspects of dependent claim 5. The rejection is traversed and reconsideration is requested.

As will be discussed below, Muller, Murray, and Merchant fail to disclose or suggest the elements of any of the presently pending claims.

Dependent claim 5 depends from independent claim 1 and recites the additional features of “a variable sized address resolution logic table; and a variable sized VLAN table, wherein said variable sized address resolution logic table and said variable sized VLAN table is in communication with said memory management unit, said at least one stack link interface, and said at least one data port interface.” Because the combination of Muller and Merchant must teach, individually or combined, all the recitations of the base claim and any intervening claims of dependent claim 5, the arguments presented above supporting the patentability of independent claim 1 over Muller and Murray are incorporated herein.

Merchant generally describes a method to enable a port of a network switch to support connections with multiple VLANs. See column 1, lines 50-55. Each multiport switch 12 includes a media access control (MAC) module 20 that transmits and receives data packets to and from 10/100 Mb/s physical layer (PHY) transceivers 16 via respective reduced media independent interfaces (RMII) 18 according to IEEE 802.3u protocol.

Each multiport switch 12 also includes a gigabit MAC 24 for sending and receiving data packets to and from a gigabit PHY 26 for transmission to the gigabit node 22 via a high speed network medium 28. See column 3, lines 38-47.

However, Merchant does not cure the deficiencies of Muller and Murray. Similarly to Muller and Murray, Merchant fails to teach or suggest, at least, “the data is removed from said at least one stack link interface in a reverse order from that in which the data is added, where the most recently added data is the first one removed,” as recited in independent claim 1. Instead, Merchant describes, at most, a frame that may include a VLAN tag header that identifies the frame as information destined to one or more members of a prescribed group of stations. See column 5, lines 45-48. A combination of Muller and Merchant would not provide for the entire claim recitations of independent claim 1, and, accordingly, dependent claim 5.

Accordingly, in view of the foregoing, it is respectfully requested that independent claim 1 and related dependent claim 5 be allowed.

CONCLUSION:

In view of the above, Applicant respectfully submits that the claimed invention recites subject matter which is neither disclosed nor suggested in the cited prior art. Applicant further submits that the subject matter is more than sufficient to render the claimed invention unobvious to a person of skill in the art. Applicant therefore

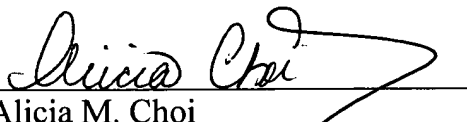
respectfully requests that each of claims 1-3, 5-12, 14-23, 25-35, 37-38, and 40-42 be found allowable and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicant respectfully petitions for an appropriate extension of time.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,


Alicia M. Choi
Registration No. 46,624

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
8000 Towers Crescent Drive, 14TH Floor
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802
AMC:jkm

Enclosures: Request for Continued Examination (RCE) Transmittal
Check No. 15406